ABSTRACT OF THE DISCLOSURE

An array of floating gate memory cells, and a method of making same, where each pair of memory cells includes a pair of trenches formed into a surface of a semiconductor substrate, with a strip of the substrate disposed therebetween, a source region formed in the substrate strip, a pair of drain regions, a pair of channel regions each extending between the source region and one of the drain regions, a pair of floating gates each disposed in one of the trenches, and a pair of control gates. Each channel region has a first portion disposed in the substrate strip and extending along one of the trenches, a second portion extending underneath the one trench, a third portion extending along the one trench, and a fourth portion extending along the substrate surface and under one of the control gates.